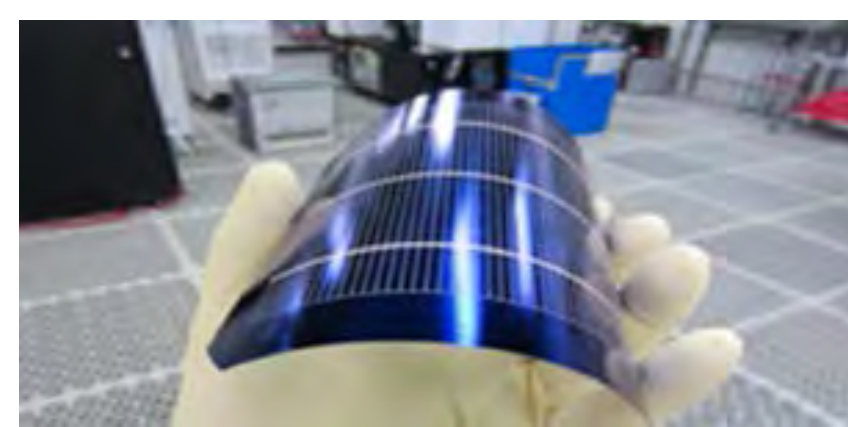


Bottom-up Module Reliability Studies at ASU

Mariana Bertoni, Govindasamy Tamizhmani, Stuart Bowden, Christiana Honsberg
Ira A. Fulton Schools of Engineering, Arizona State University, Tempe, AZ, 85287

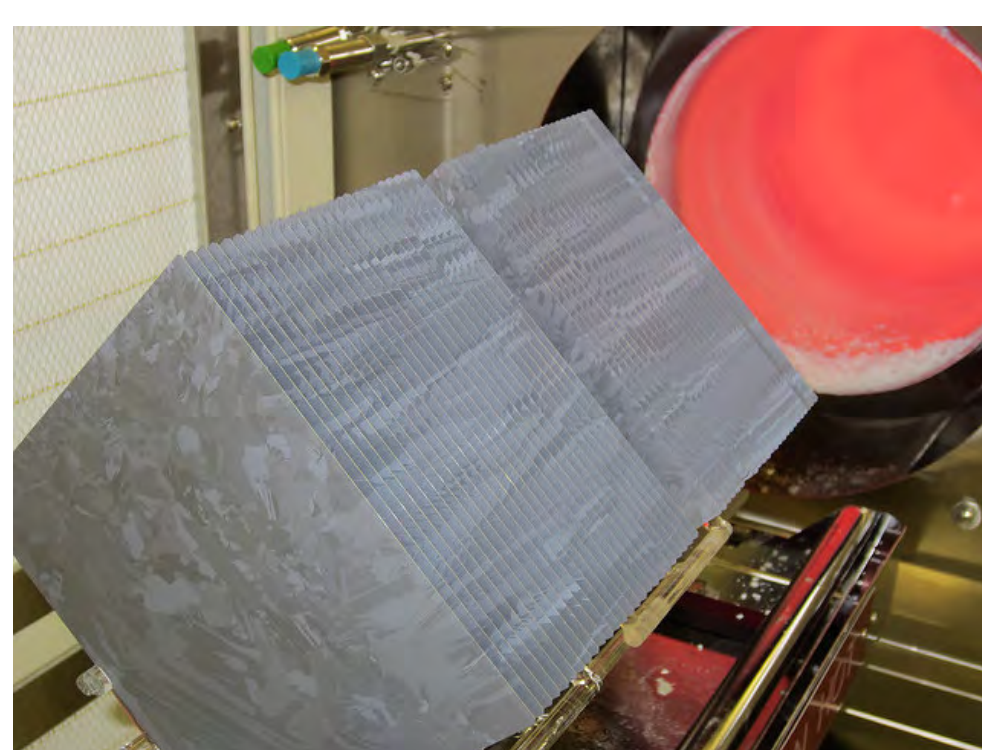
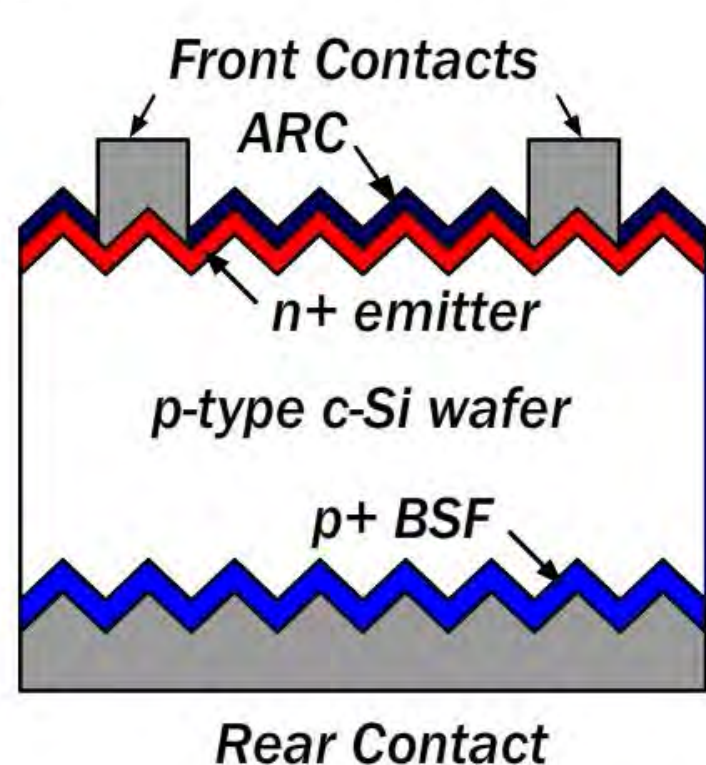
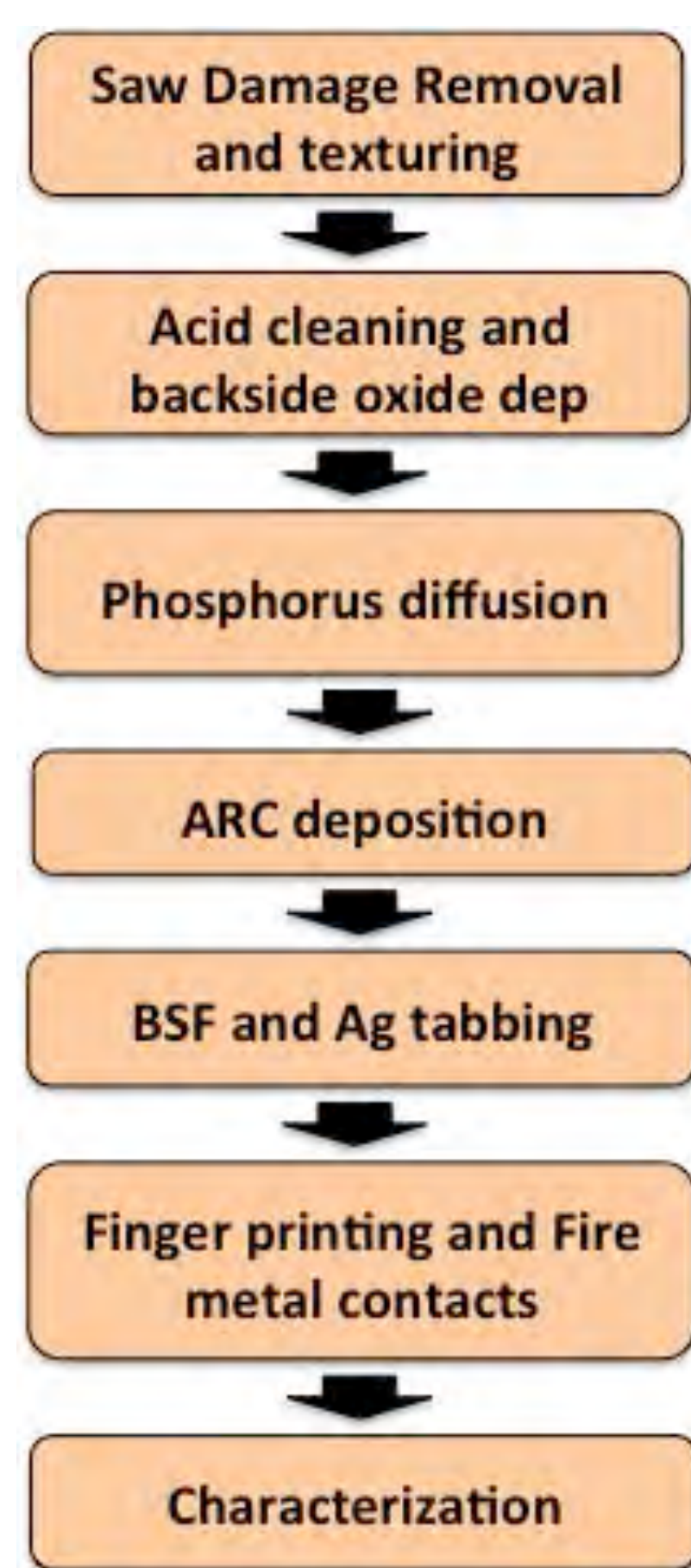
Introduction

- 6" Silicon process line for diffused and heterojunction cells
- Bottom-up Evaluation of:
 - Materials
 - Processing steps
 - Encapsulants
 - Lamination



Pilot Lines

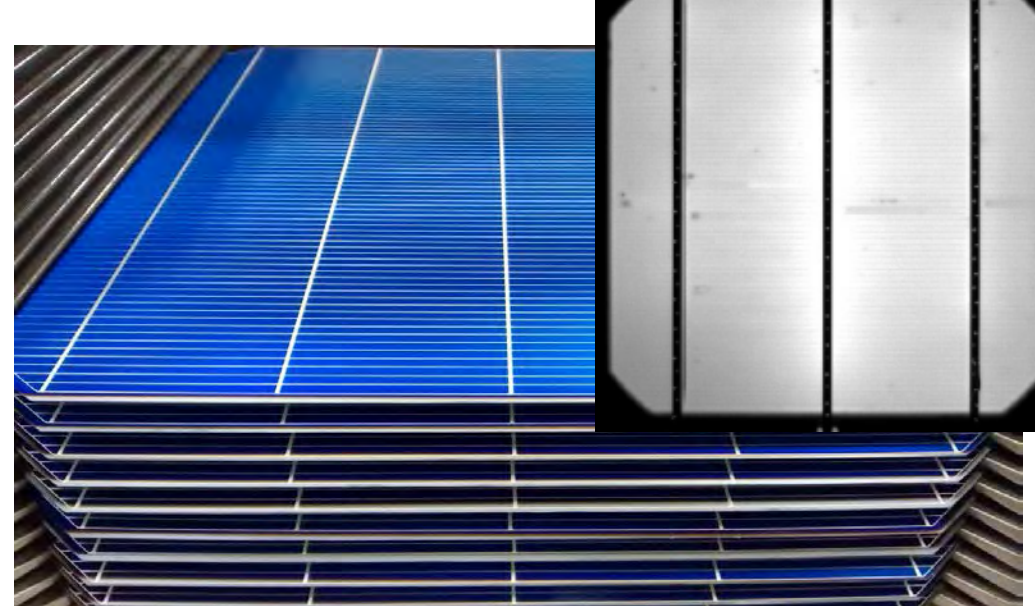
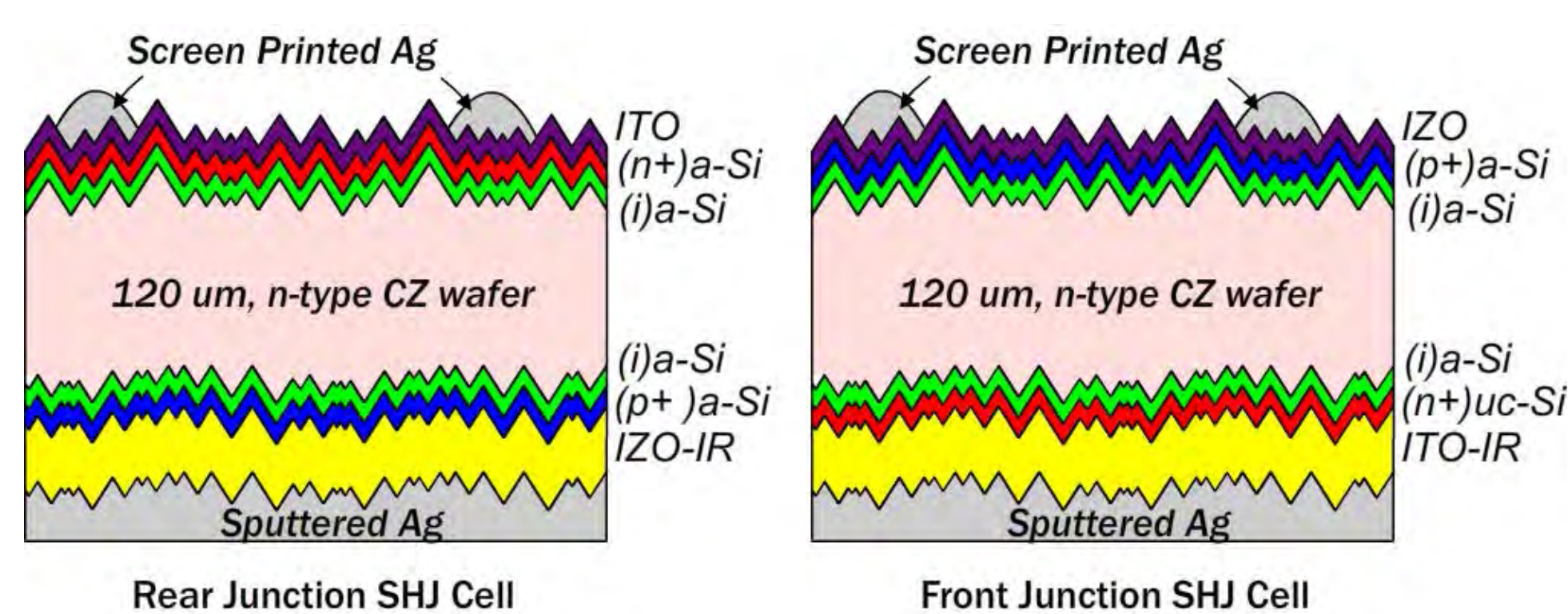
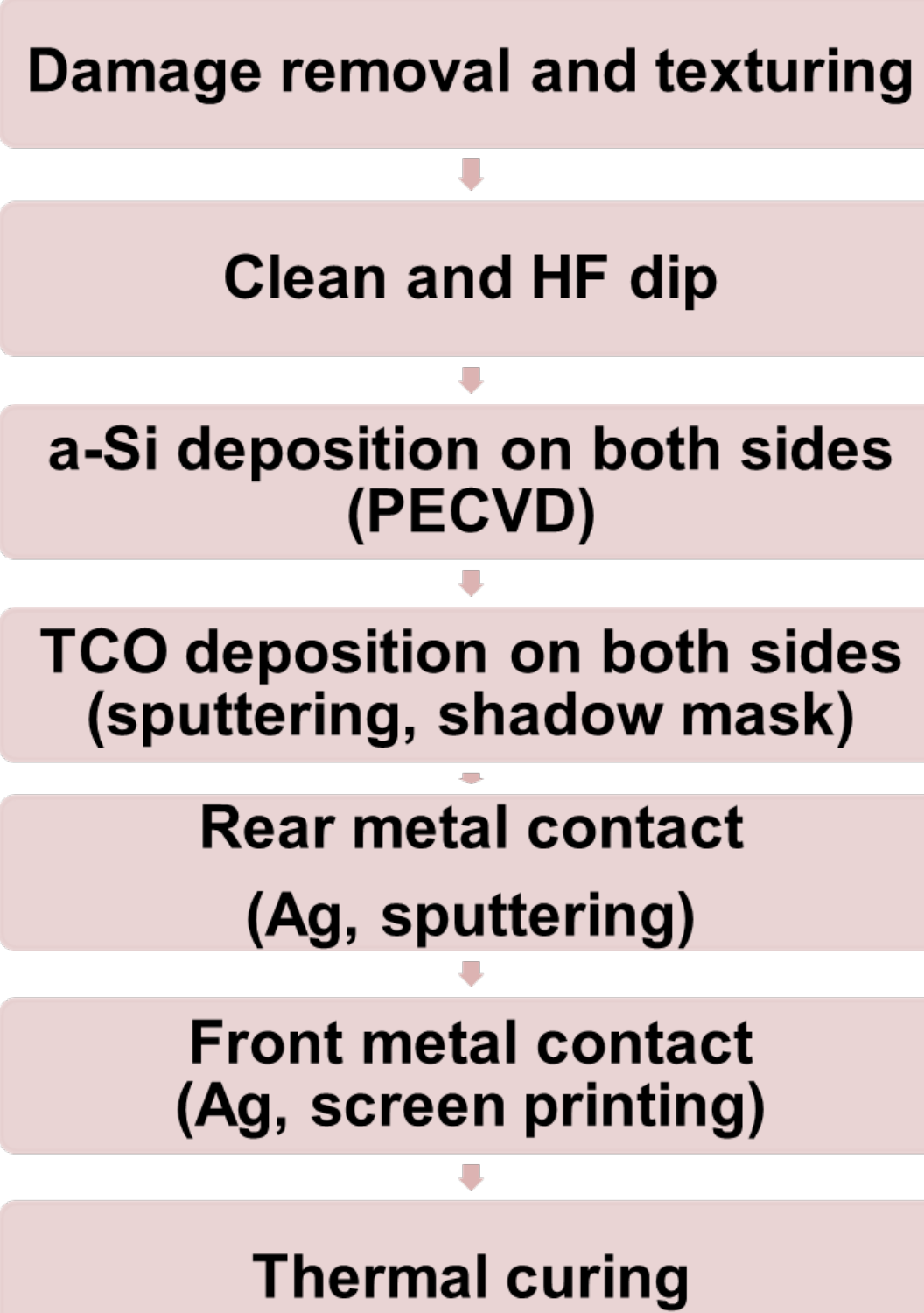
➤ Diffused Junction Cell Line



V_{oc} (mV)	J_{sc} (mA/cm ²)	FF(%)	Eff. (%)	Area (in)
362	36.7	79.8	18.6	6x6

➤ HIT Cell Line

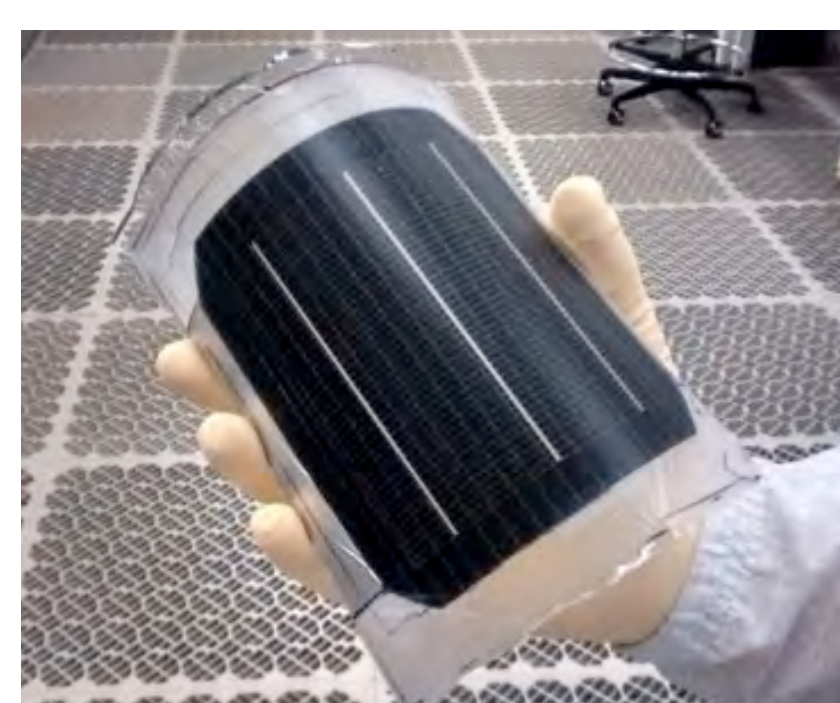
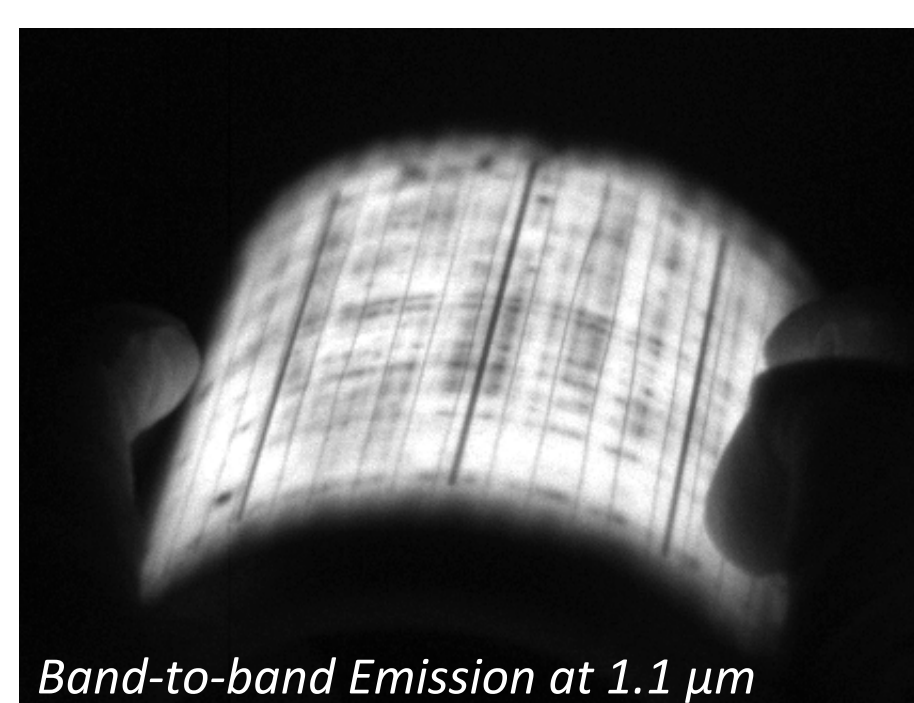
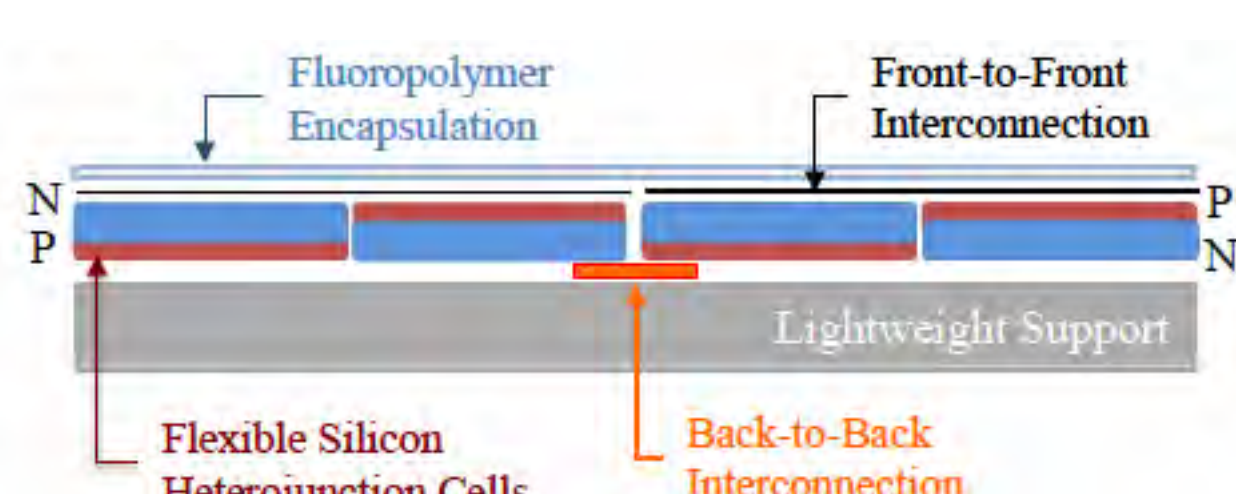
SHJ Solar Cell Process Flow



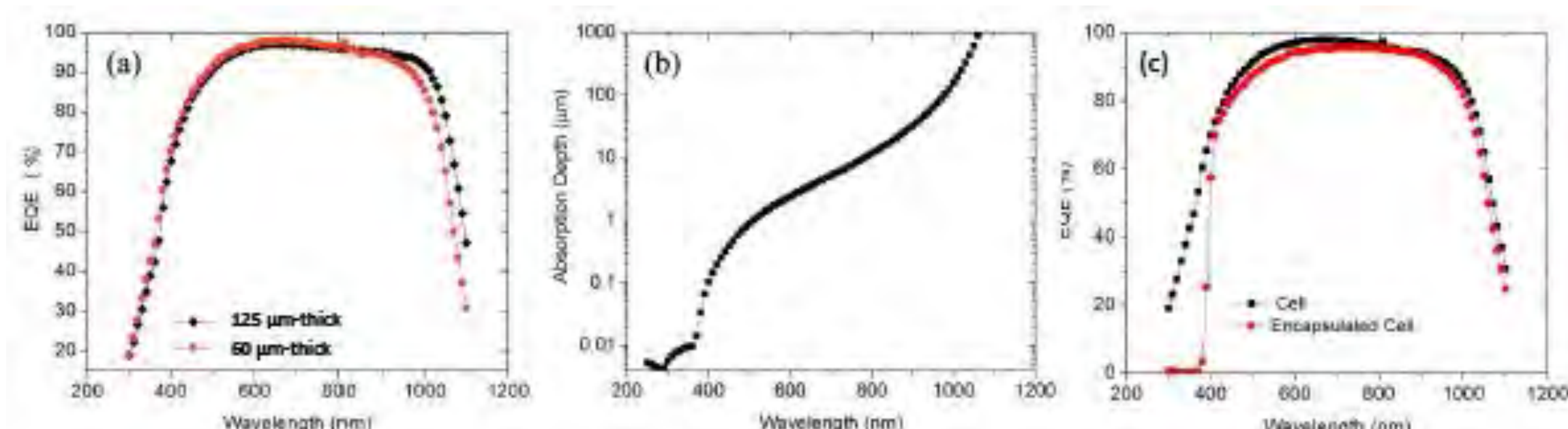
V_{oc} (mV)	J_{sc} (mA/cm ²)	FF(%)	Eff. (%)	Area (cm ²)
727	38.7	78.2	22.0	239

➤ Flexible Silicon Cells

Encapsulated using Fluoropolymer foil
Front-to-front and front-to-back intercon.

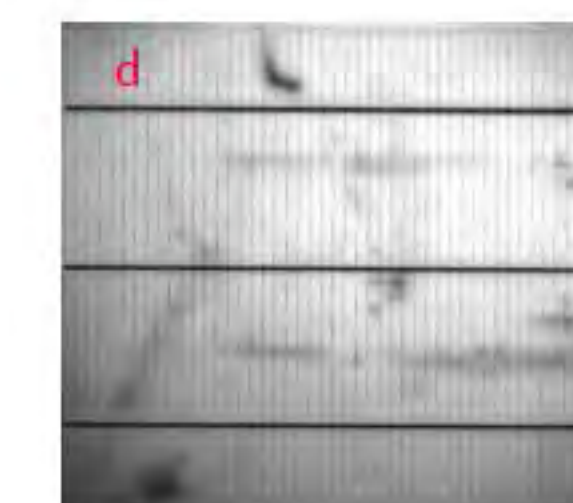
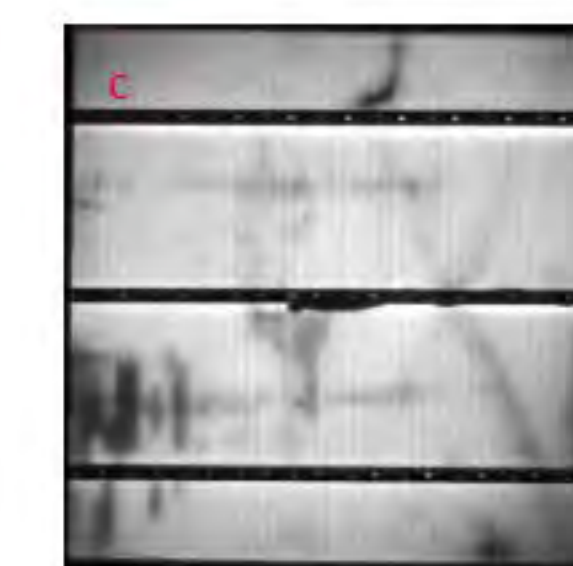
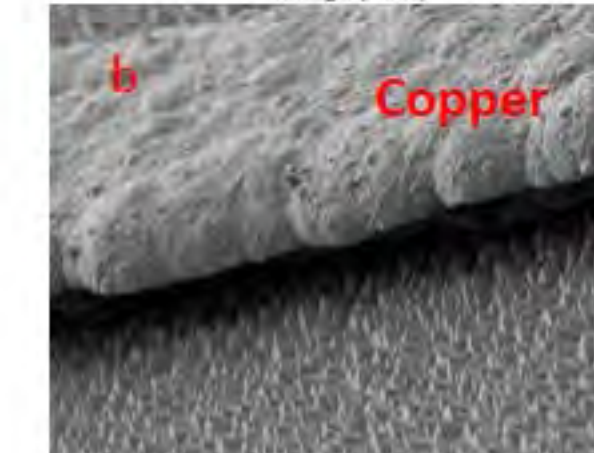
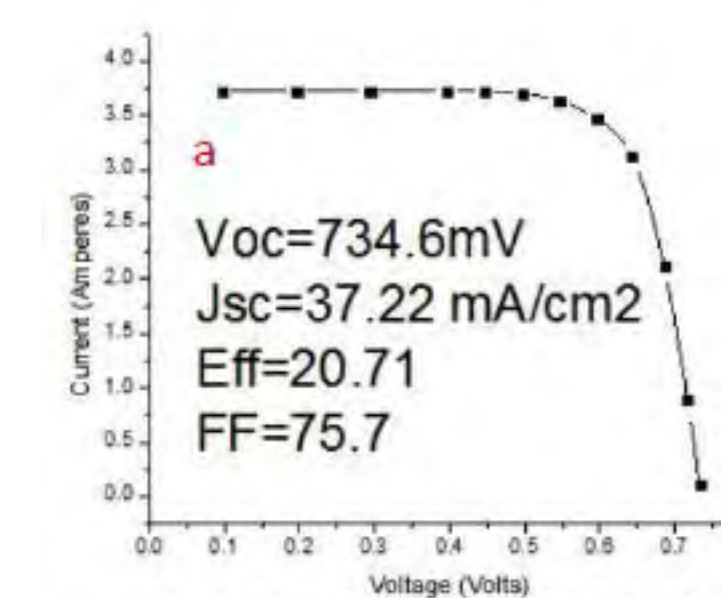


- (a) EQE 125um and 60um cell
- (b) Absorption depth in Si
- (c) 60 um-thick cell before and after encapsulation



Advanced Processing

➤ Copper, Nickel and Tin plating



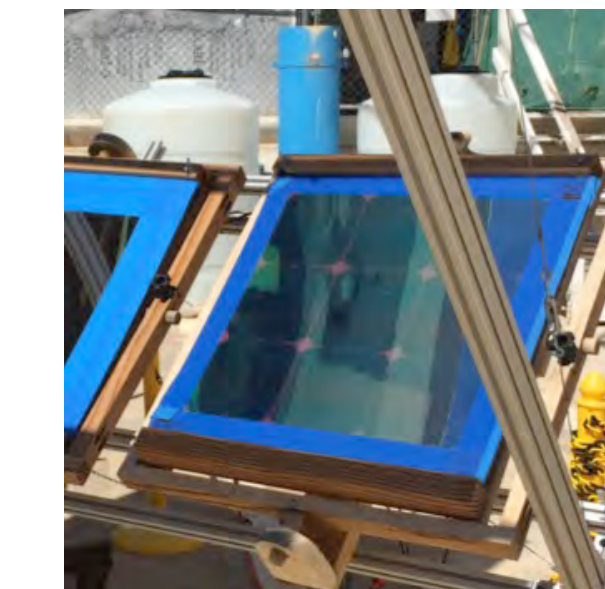
(a) IV Bifacial Electroplated Cell, (b) SEM, (c) EL, (d) PL

Lamination

➤ Standard and Unconventional Modules

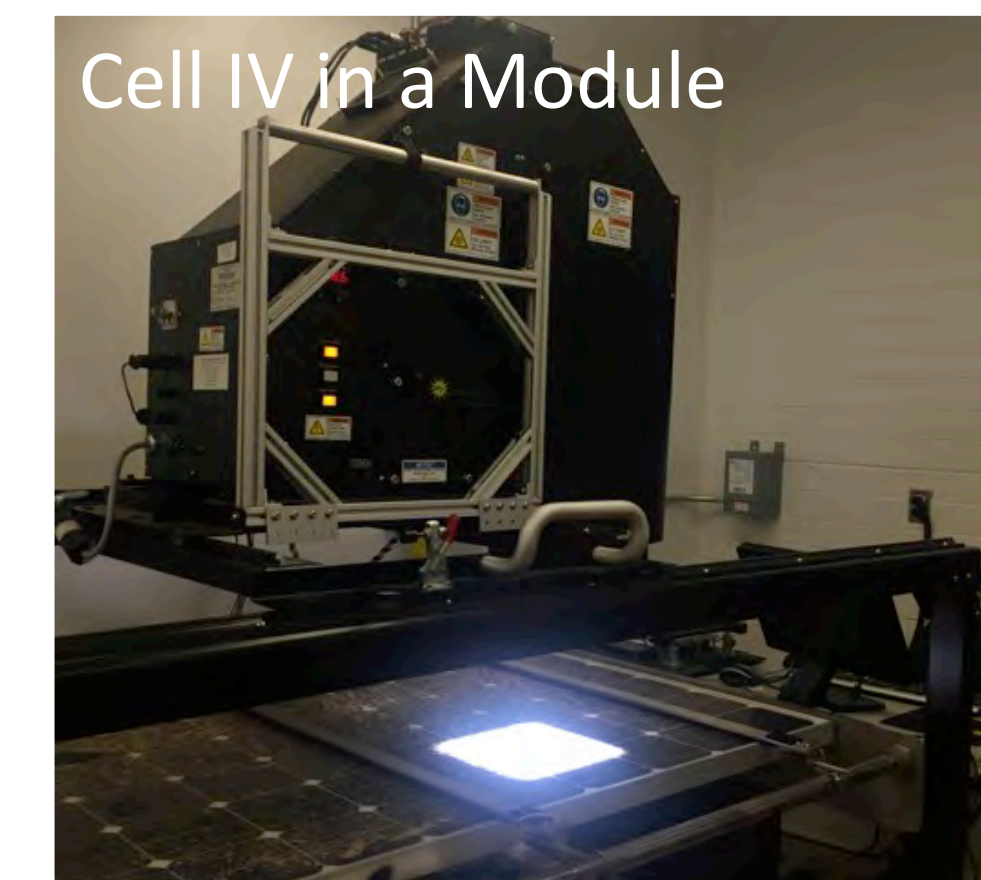
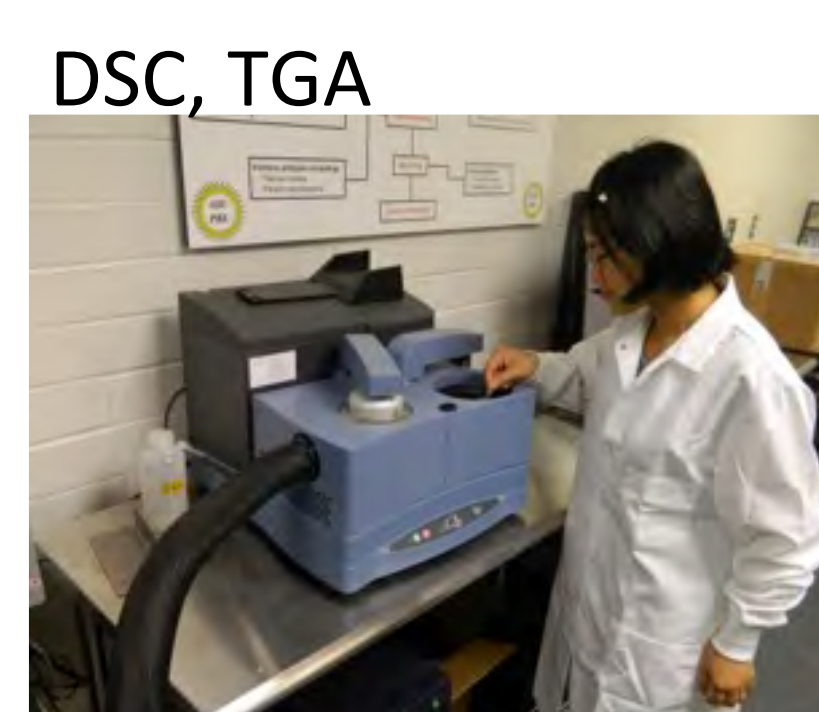


- 20% Cells
- 18% Modules
- Suns V_{oc} characterization



Characterization @ PRL

➤ Indoor Testing



➤ Outdoor Testing



➤ Accelerated Testing and Modeling

Walk-in UV chamber
Modeling: ReliaSoft, Pvsyst, Minitab, Tableau, SAS, JMP
PID Test station: Module and Cell



UV weathering



PRL Mission

